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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,716	06/08/2000	Stephen V. Kosonocky	YO999-369	9798

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William E Lewis
Ryan & Mason LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/589,716	KOSONOCKY, STEPHEN V.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "^[p(n)*C(n-1)]*[p(n)+C(n-1)]" must be shown or the feature(s) canceled from the claim 2 line 2. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

In the abstract, the applicant is advised to remove the term "1500-44.APP" in line 7.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 2, the limitation "the binary output signal S(n)" in line 1 lacks an antecedent basis. The examiner considers this limitation "the binary output signal S(n)" as "a binary output signal S(n)". In addition, the recitation "S(n)" is represented by an expression "^[p(n)*C(n-1)]*[p(n)+C(n-1)]" is indefinite as whether the binary output signal S(n) must be computed according to the above expression or only satisfied the above expression. For examination purposes, the examiner considers the binary output signal S(n) is to satisfy the above expression. Thus, claims 3-5 are also rejected under the same rationale for being dependent on the rejected claim 2.

Re claim 6, the limitation "the need" in line 16 lacks an antecedent basis. The examiner considers this limitation "the need" as "a need". Claims 13 and 20 have the same problem. Thus, claims 7-12 and 14-19 are also rejected under the same rationale for being dependent on the rejected claims 6 and 13 respectively.

Re claim 7, the limitations "a" in line 4 and "b" in line 5 lack an antecedent basis. The examiner considers this limitation "a" in line 4 and "b" in line 5 as "a_i" and "b_i" respectively. Claim 14 has the same problem.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (U.S. 3,646,332).

Re claim 1, Suzuki discloses an apparatus for use in summing at least two binary values (binary A and B) in Figures 4 and 8 comprising a binary adder circuit (Figure 8) responsive to a first binary value (A), a second binary value (B), and a carry value (C or output of 5) and operative to generate a binary output value (S or sum or output of 12) representative of a summation of the first binary value the second binary value and the carry value the binary adder circuit having logic for implement an exclusive OR function (2' with Figure 4 as the logical structure of EXOR and col. 3 lines 16-20) that generates the binary output value without one of appositive and a negative complementary version of the carry value (only C is inputted to component 2' to compute the sum).

Re claim 2, Suzuki further discloses the binary output signal S(n) is satisfied by an expression: ^(p(n)*C(n-1)*(p(n)+C(n-1)).

7. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. 5,905,667).

Re claim 1, Lee discloses an apparatus for use in summing at least two binary values (A and B) in Figure 3 comprising a binary adder circuit respective to a first binary value (A) a second binary value (B) and a carry value (C) and operative to generate a binary output value (SUM) representative of a summation of the first binary value the second binary value and the carry value the binary adder circuit having logic for implement an exclusive OR function (MP33, MP34 and col. 1 lines 41-45) that generates the binary output value without one of appositive and a negative complementary version of the carry value (only C is applied to 31 and 33).

Re claim 2, Lee further discloses the binary output signal S(n) is satisfied by an expression: ^(p(n)*C(n-1)*(p(n)+C(n-1)) wherein C(n-1) is a generate signal from a binary value n-1 associated with the carry value, p(n) is a propagate signal associated with the first binary value and the second binary value, ^ is a logical complement operator, * is an AND operator, and + is an OR operator.

Re claim 3, Lee further discloses the logic of the binary adder circuit in Figure 3 comprising a first NMOS transistor stage (left portion of 31) for performing an AND operation on the generate signal (C) and the propagate signal (parallel NMOS A and B); an inverter stage (MP31), coupled to the first NMOS transistor stage for inverting an output signal generated by the first NMOS transistor stage (CARRY'); a second NMOS transistor stage (left lower portion of 33 wherein A, B, and C are structured in parallel)

for performing an OR operation on the generate signal (C) and the propagate signal (parallel NMOS and B); and a NOR gate (other portion of 33 and 34), coupled to the inverter stage (31) and the second NMOS transistor stage (left lower portion of 33), for combining an output signal generated by the inverter stage and an output signal generated by the second NMOS transistor stage to generate the binary output value.

Re claim 4, Lee further discloses in Figure 3 the first NMOS transistor stage is responsive to more than one generate signal (C) and more than one propagate signal (A and B).

Re claim 5, Lee further discloses in Figure 3 the second NMOS transistor stage is responsive to more than one generate signal (C) and more than one propagate signal (A and B).

8. Claims 6-9, 11, 13-16, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jiang et al. (U.S. 5,943,251).

Re claim 6, Jiang et al. disclose an N-bit parallel adder (col. 8 line 10) in Figure 7 comprising: a first logic stage configured to receive a first N-bit binary value and a second N-bit binary value and compute generate signals and propagate signals for each bit (P0G0-P35G35); a second logic stage coupled to the first logic stage (30-38) configured to compute block generate signal ($G^4_0 - G^4_8$) and block propagate signals ($P^4_0 - P^4_8$) for groups of one through m (m = 9) bits from the generate (G0-G35) and propagate (P0-P35) signals computed in the first logic stage; a third logic stage (40-42) coupled to the second logic stage (30-38) configured to combine the block generate and

block propagate signals of one set of groups with the block generate ($G^{12}_0 - G^{12}_0$) and block propagate signals of another set of groups ($P^{12}_0 - P^{12}_0$); and a fourth logic stage (40) coupled to the third logic stage (40-42) configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal (Figure 8) wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without the need for one of positive and negative complementary signal generation (Figure 7 and equations 3-7 in col. 1).

Re claim 7, Jiang et al. further disclose a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i (col. 2 line 43), wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$ where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i (col. 1 equation 1) where a represents the first binary value and b represents the second binary value, and where p represents the propagate signal (col. 1 equation 2) and is equivalent to a logical summation operation between a_i and b_i.

Re claim 8, Jiang et al. further disclose in Figure 7 the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals (equation 7 in col. 1 wherein Ci is in col. 2 line 43).

Re claim 9, Jiang et al. further discloses in Figure 7 the fourth logic stage implements an exclusive OR function to generate the summation signal (col. 4 lines 16-17).

Re claim 11, Jiang et al. further disclose N is equal to 64 (col. 8 line 10 N = 64).

Re claim 13, it is the method claim of claim 6. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 14, it is the method claim of claim 7. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 15, it is the method claim of claim 8. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 16, it is the method claim of claim 9. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 18, it is the method claim of claim 11. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 20, it is the device claim of claim 6. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 6.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Jiang et al. (U.S. 5,943,251) in view of Lee (U.S. 5,905,667).

Re claim 12, Jiang et al. do not disclose the logic stages are implemented with complementary metal oxide semiconductor components. However, Lee discloses in

Figure 3 the logic stages are implemented with complementary metal oxide semiconductor components (31 and col. 1 lines 37-42). Therefore, it would have been obvious to a person having ordinary skill in the prior art at the time the invention is made to implement the logic stages disclosed by Jiang et al. with complementary metal oxide semiconductor components because it would enable to generate the complemented signal for computing the sum of two or more binary numbers and reduce the power consumption.

Re claim 19, it is the method claim of claim 12. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 12.

Allowable Subject Matter

11. Claims 10 and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,257,218 to Poon discloses a parallel carry and carry propagation generator apparatus for use with carry-look-ahead adders.

b. U.S. Patent No. 4,718,034 to takla et al. disclose a carry-save propagate adder.

c. U.S. Patent No. 5,793,662 to Duncan et al. disclose a null convention adder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

March 10, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100